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# METHOD AND DEVICE FOR PRODUCING DELAYED SIGNALS

## FIELD OF THE INVENTION

The present invention relates to a method and a device for producing an output signal that is delayed compared to an input signal. In particular the invention relates to a method and a device for producing a plurality of output signals that are in each case delayed by a defined phase angle compared to an input signal, and that have a mark-to-space ratio of for example 50%.

## BACKGROUND OF THE INVENTION

For the purposes of data recovery by oversampling, many versions of an input timing signal delayed in each case by identical times or phase angles are required, with which in each case various sampling elements can be controlled. In order not to let the number of signals become too high, it is desirable to be able to initiate a sampling procedure with the rising edge as well as with the falling edge of each signal. For this purpose it is necessary that the signals have an accurately defined mark-to-space ratio, in particular a mark-to-space ratio of 50%.

In order to delay the input timing, delay elements are generally employed. On account of process-conditioned differences between the components in the delay elements the mark-to-space ratio deviates from the desired value however, for example by 50%. This deviation becomes increasingly larger in the course of a chain

of delay elements since the errors to some extent add up. In addition there is the deviation that arises if the input signal of the chain already deviates from the desired value, for example by 50%.

With a relatively large number of delay elements the mark-to-space ratio at the end of the chain deviates to such an extent from the desired value that it is no longer possible to use the rising edge as well as the falling edge of the signal since the result would be too inaccurate.

In principle it would if necessary be possible to regulate the mark-to-space ratio actively. This means however a high switching expenditure in the case of high frequencies in some cases above 1 GHz, as are required for oversampling at high data rates.

One object of the present invention is accordingly to provide a method and a device with which a signal that is delayed compared to an input signal can be generated with an accurate predetermined mark-to-space ratio.

## SUMMARY OF THE INVENTION

According to the invention it is proposed to form at least two intermediate signals that are delayed by different amounts compared to an input signal and then to combine a first intermediate signal and a second intermediate signal different therefrom, of these intermediate signals, to form an output signal, in such a way that a rising edge of the output signal corresponds to a rising or falling edge of the first intermediate signal and a falling edge of the output signal corresponds to a rising or falling edge of the second intermediate signal. The mark-to-space ratio of the output signal is thereby defined by the delay between the first and the second intermediate signal. The delayed intermediate signals are preferably formed by a delay chain, i.e. by successive delay of the input signal. In order to form a plurality of output signals delayed in each case by the same times with a mark-to-space of 50%, 2k(k=1,2...) successive intermediate signals delayed substantially by 360°/(2k) compared to the input signal are preferably formed. Those intermediate signals whose delay with respect to one another is substantially 180° are then combined in each case to form an output signal. These signals may be combined for example by a multiplexer, in particular in such a way that the respective multiplexer forms, depending on a control signal, the first intermediate signal or the second intermediate signal in inverted form as the output signal. A further one of the intermediate signals may be used in this connection as control signal. For a mark-to-space ratio of 50% an intermediate signal may be used that has an absolute delay of substantially 90° with respect to the first as well as to the second intermediate signal, i.e. lies exactly between the first and the second intermediate signal. In order to obtain a greater accuracy of the emitted output signal, it is advantageous to employ a regulation in the form of a delay regulation loop

or delay-locked loop (DLL). In this connection the delay of the intermediate signal is regulated so that the intermediate signal with the greatest delay experiences a delay of substantially 360° with respect to the input signal. In this way when the delay chain described above is used the overall delay remains constant and a process variability of the individual delay elements is partially compensated.

The method according to the invention and the device according to the invention have the advantage that the delay caused by delay elements reacts less sensitively to the process variability than does the mark-to-space ratio. Since the mark-to-space ratio of the output signal is defined in the present invention by the delays of the intermediate signals, the mark-to-space ratio can thus be accurately adjusted.

## BRIEF DESCRIPTION OF THE DRAWINGS

The invention is described in more detail hereinafter with reference to the accompanying drawings, in which:

Fig. 1 is a circuit diagram of an example of implementation of a device according to the invention,

Fig. 2 is an enlarged section of the circuit diagram shown in Fig. 1,

Fig. 3 are examples of signal waveforms,

Fig. 4 is a block diagram of a delay locked loop according to the invention, and

Fig. 5 shows the waveform of regulating signals depending on the delay of the intermediate signals in the delay locked loop illustrated in Fig. 4.

## DETAILED DESCRIPTION

The circuit diagram of a device according to the invention is illustrated in Fig. 1.

When the circuit is in operation an input timing signal is fed to a connection 34. The timing signal is delayed by a chain of nominally identical delay elements 1 to 19. For reasons of space the chain of delay elements 1 to 19 is shown folded, whereas for the actual implementation it is preferably realised in extended form, in which the lines corresponding to one another should as far as possible all be equally long and symmetrical.

Multiplexers 20 to 30 and buffers 33 are connected up to the delay elements 1 to 19 as shown in Fig. 1. The delayed output signals can be tapped at the outputs 35 of the multiplexers 23 to 30.

The first two delay elements 1 and 2 of the delay chain serve to form pulses. So that the zero passages have regular interspacings at all outputs 35, the signals within the chain should all have the same shape. Due to the combination of amplification and band limitation, in a chain of identical stages such a shape is already formed after a few stages, in the present case two stages, by the delay elements. So that all stages are actually identical, they must also be loaded identically. For this reason the multiplexers 20 and 21 and buffer stages 33 are also present when their output signals are not used. In the present example of implementation the loading due to these elements changes only slightly however when they are connected in a currentless manner. This is therefore effected in all

elements, for example in the multiplexers 20 and 21, whose output signals are not used in the circuit. The actual input signal for the production of the delayed output signals is present at the output of the delay element 2.

The actual chain consists of the 16 delay elements 3 to 18. So that the last delay element 18 of this actual chain experiences the same load as the remaining elements 3 to 17, a delay element 19 is additionally present as load at the end of the chain. In the illustrated example of implementation the nominal delay of each delay element is preferably 22.5° or 1/16 of a period, so that overall a delay of around 360° is achieved by the delay elements 3 to 18. In order to produce the output signals that are to be tapped at the outputs 35, in each case two delayed signals are combined by the multiplexers 23 to 30 to form a respective output signal.

The interconnection of the multiplexers 23 to 30 is shown on an enlarged scale in Fig. 2 with the example of the multiplexer 24. In the illustrated section the signal after the delay element 4 is present at a first input 37 and the signal after the delay element 12 is present at a second input 38. In this connection the circuit connections are such that the signal after the delay element 12 is present inverted at the multiplexer 24, which may be effected in this case with differential signals by simply transposing the lines. Eight delay elements, i.e. half of the actual chain, thus lie between the two signals present at the inputs 37 and 38. In the example discussed above, in which each delay element produces a delay of 22.5°, this means a delay of around 180° between the signal present at the input 37 and the signal present at the input 38.

In addition a control signal is fed to the multiplexer 24 at a control input 36, which signal is tapped after the delay element 8, i.e. exactly halfway between the delay element 4 and the delay element 12.

Possible signal waveforms at the inputs 36 to 38 and at the output 35 of the multiplexer 24 are shown in a time-dependent manner by way of example in Fig. 3.

In this connection ZS1 denotes the first intermediate signal tapped after the delay element 4 which is fed to the multiplexer 24 at the input 37, and ZS2 denotes the second intermediate signal tapped after the delay element 12 which is then fed in inverted form to the second input 38 of the multiplexer. The intermediate signals ZS1 and ZS2 have a phase shift of 180° with respect to one another.

In addition a control signal SS is formed, which is tapped after the delay element 8 and is fed to the multiplexer at its control input 36. This is displaced by 90° with respect to the first intermediate signal ZS1 and is in advance of the second intermediate signal ZS2 by 90°. The multiplexer combines the first intermediate signal ZS1 and the second intermediate signal ZS2 now in such a way that, if the control signal has a logic value 0, the first intermediate signal ZS1 produces the output signal, whereas if the control signal SS has a logic value 1, the second intermediate signal ZS2 in inverted form forms the output signal. The waveform of the output signal is shown by AS in Fig. 3.

In the illustrated example the intermediate signals ZS1 and ZS2 that are formed from the input signal have a mark-to-space ratio that differs by 50%. The output signal AS has on the other hand a mark-to-space ratio of 50%. This is

achieved by the delay of the intermediate signal ZS2 compared to the intermediate signal ZS1 of 180°, and of the control signal SS compared to the intermediate signal ZS1 of 90°. The control signal SS controls the multiplexer 24 so that a rising edge of the intermediate signal ZS1 results in a rising edge of the output signal AS, whereas a rising edge of the intermediate signal ZS2 results in a falling edge of the output signal AS.

In principle however other delays between the intermediate signals and the control signal are also conceivable in order to produce an output signal with a different desired mark-to-space ratio. In addition the circuitry may also be designed so that in each case the falling edges of the intermediate signals ZS1 and ZS2 determine the position of the edges of the output signal AS.

It should also be noted in this connection that the frequency is not altered by the combination of the signals ZS1 and ZS2, i.e. the output signal AS has the same frequency as the intermediate signals ZS1 and ZS2 produced from the input signal. The mark-to-space ratio however can be adjusted due to the delay.

Fig. 1 additionally shows a phase detector 31 that controls a charge pump 32. The charge pump in turn controls the delay of the delay elements 1 to 19. The control lines required for this purpose are for reasons of clarity not shown in Fig. 1. This arrangement forms a delay regulation system (delay locked loop, DLL). Preferably the regulation is performed in such a way that overall a delay of 360°, i.e. a complete period, is achieved through the delay elements 3 to 18. In this way a rising edge of the input signal present at the delay element 3 of the actual delay chain covers a rising

edge of the signal present after the delay element 18. In the illustrated example of implementation the phase detector 31 receives as input signal the signal before the delay element 3, i.e. the input signal of the actual delay chain (which consists of the delay elements 3 to 18), an intermediate signal that is tapped after the delay element 6, i.e. after a quarter of the chain, and the intermediate signal after the delay element 18, i.e. at the end of the chain. These signals are fed to the phase detector 31, in each case via buffers 33.

Fig. 4 shows an example of implementation of a delay regulation system such as may be used for example in the example of implementation illustrated in Fig. 1.

In Fig. 4 the delay chain of Fig. 1 is shown in simplified form. For the simplified representation in each case four delay elements of the actual delay chain consisting of the delay elements 3 to 18 are shown combined as delay blocks 40, 41, 42 and 43. Each of these delay blocks delays the signal nominally by a quarter period, or by 90°. An input signal 39 is fed to this delay chain, the signal corresponding in Fig. 1 to the signal present before the delay element 3. The phase detector 31 substantially comprises three logic elements, an NOT element 45 and two AND elements 46 and 47. The input signal 39, the intermediate signal at the end of the delay chain, i.e. with the largest delay, after the delay block 43 and a further intermediate signal after the delay block 40 are fed to the phase detector. Two delay regulation signals are generated by the logic elements 45 to 47. The AND element 46 emits a first delay regulation signal ("down signal") which indicates that the overall delay should be corrected downwardly. The AND element 47 emits a second delay regulation signal ("up signal") that specifies that the overall delay of the delay chain

should be corrected upwardly. Depending on the supplied signals, the delay regulation signals appear as illustrated in the following table:

| Input Signal | Further Intermediate Signal | Intermediate Signal with Greatest Delay | First Delay Regulation Signal | Second Delay Regulation Signal |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 |

These delay regulation signals are passed on further by an element 48 to the charge pump 32. The charge pump 32 in turn controls the delay blocks 40 to 43 and the delay elements 1 to 19. This control and regulation is carried out in such a way that the overall delay of the delay elements 40 to 43 is 360°. Since the delay elements are nominally identical, the delay of each individual delay element 40 to 43 is substantially 90°, and of each individual delay element 1 to 19 is substantially 22.5°.

The characteristics of the phase detector are shown in Fig. 5. The waveforms of the delay regulation signals and of an overall or effective delay regulation signal resulting therefrom are shown as a function of the delay of a delay block.

In each case the on period of the delay regulation signal is plotted in relation to the period duration over the phase delay of a delay block with four delay elements, in which the characteristic line (i) corresponds to the first delay regulation signal, the

characteristic line (ii) corresponds to the second delay regulation signal and the characteristic line (iii) corresponds to the effective or overall delay regulation signal resulting therefrom.

It should be noted that the linear waveform of the overall delay regulation signal is around 90° or 0.25. This means a regulation to the value of 0.25 or 90° for the individual delay blocks. The phase detector delivers a signal of correct polarity up to at least approximately double the nominal delay. Due to production variations it could happen that the unstable operating point of the system in the case of double the nominal delay becomes a stable operating point. The output signal of the phase detector is proportional to the deviation as long as the delay deviates less than a third of the nominal value.

It should be noted that in principle other forms of embodiment of the delay locked loop are of course also conceivable. Due to the fact that the overall delay is regulated to 360°, process deviations of the individual delay elements are less strongly manifested in the output signal.